
CS5333 to CS5340 Conversion

by Kevin L Tretter

1. Introduction

The CS5333 and CS5340 are complete stereo analog-to-digital converters for digital audio systems. These converters perform sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right channels. These small, low power converters are ideal for systems requiring wide dynamic range and low noise such as set-top boxes, A/V receivers, DVD-karaoke players, DVD recorders, and automotive applications. The CS5333 is no longer recommended for new designs, and the CS5340 is the suggested replacement.

This application note identifies the implementation differences between these two devices, including:

- Key specifications
- Pinout differences
- Startup mode selections
- System clocking
- Input filter topology
- Reference pin decoupling

2. Key Specifications

Table 1 shows a comparison of the key specifications of these two devices, and Table 2 shows the pin comparison between the CS5333 and the CS5340. Although these two devices are not pin compatible, they are very similar in terms of overall functionality and feature set. The CS5340 achieves higher analog performance and supports a wider range of output sample rates, including 192 kHz. This additional performance is the main reason for the increased power consumption of the CS5340 relative to the CS5333.

Parameter	CS5333	CS5340	Units
Conversion	24	24	Bits
Dynamic Range (A-weighted)*	95	98	dB
THD+N*	-88	-95	dB
Analog Core Power Supply (VA)	+1.8 to +3.3	+3.3 to +5.0	V
Digital Core Power Supply (VD)	Powered from VA	+3.3 to +5.0	V
Digital Interface Power Supply (VL)	+1.8 to +3.3	+1.8 to +5.0	V
Maximum Power*	31	100	mW
Maximum Sample Rate	100	200	kHz
Package	16-pin TSSOP	16-pin TSSOP	
* All performance/power measurements taken with all supplies set to 3.3 V			

Table 1. Comparison of Key Specifications

The CS5333 and CS5340 are both available in a 16-pin TSSOP package. As can be seen from Table 2, all but three pins correlate directly in terms of functionality. These three pins account for a difference in operational mode selection and a separate voltage supply pin for the CS5340 digital core.

CS5333		CS5340		Description
Pin Number	Pin Name	Pin Number	Pin Name	
1	VL	3	VL	Logic Power
2	MCLK	2	MCLK	Master Clock
3	SCLK	7	SCLK	Serial Clock
4	SDATA	4	SDOUT	Serial Data
5	VA	13	VA	Analog Power
6	GND	5	GND	Ground Reference
7	LRCK	8	LRCK	Left/Right Clock
8	DIV	-	-	Speed Mode Select/MCLK Divider
9	DIF	-	-	Digital Interface Format Select
10	TST	-	-	Test Pin
11	FILT+	15	FILT+	Voltage Reference
12	REF_GND	14	REF_GND	Ground Reference
13	AINR	12	AINR	Right Channel Analog Input
14	AINL	10	AINL	Left Channel Analog Input
15	VQ	11	VQ	Quiescent Voltage Reference
16	RST	9	RST	Reset
		1	M0	Mode Selection
		6	VD	Digital Power
		16	M1	Mode Selection

Table 2. Pin Compatibility Between the CS5333 and CS5340

3. Typical Connection Diagrams

Figures 1 and 2 illustrate the typical connection diagram for the CS5333 and CS5340 respectively. The analog and digital core of the CS5333 are powered from VA, which can be set from 1.8 V to 3.3 V. The VL supply pin powers the digital interface logic from 1.8 V to 3.3 V and can be set independently from VA.

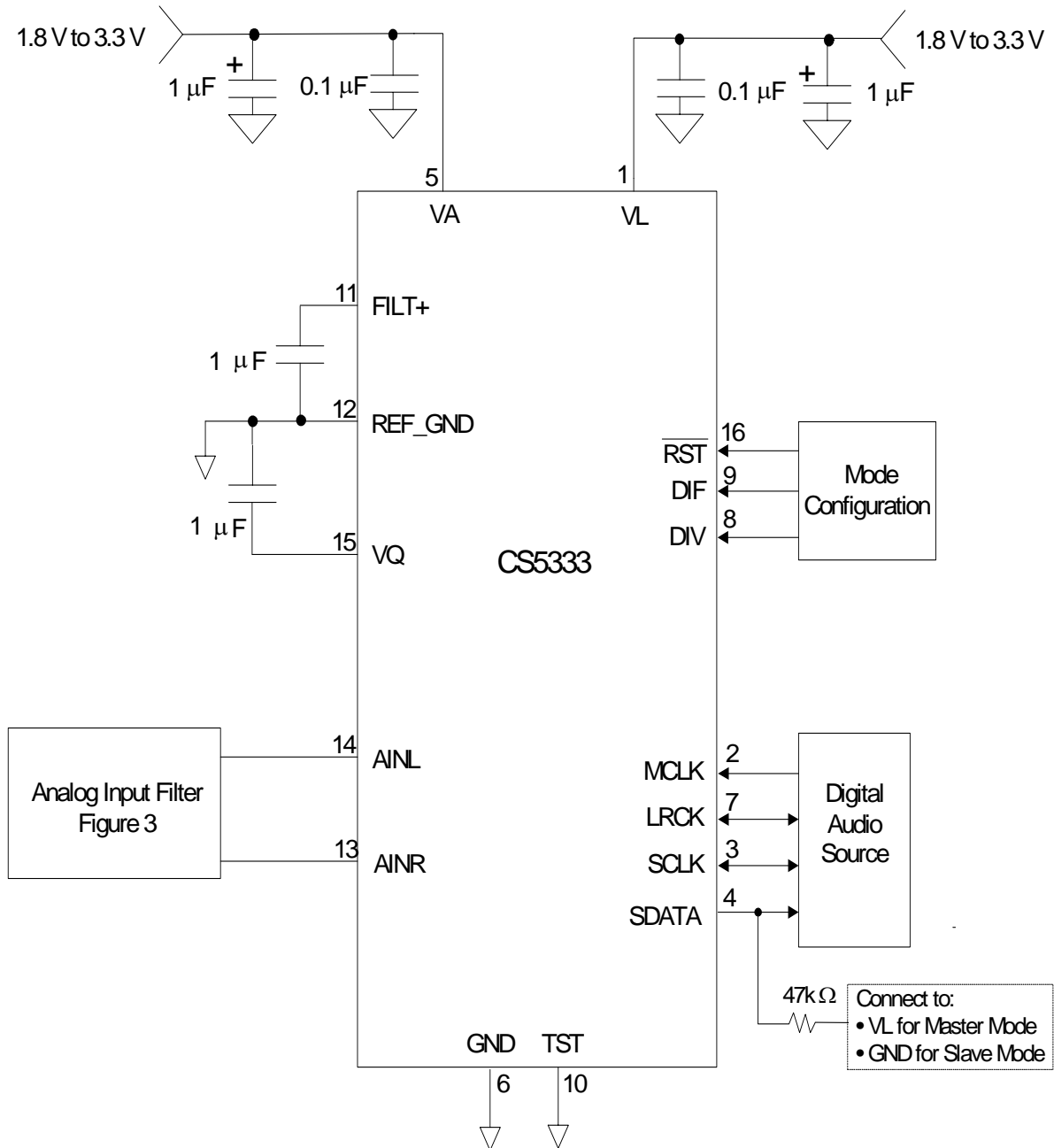


Figure 1. CS5333 Typical Connection Diagram

The CS5340 has separate power supply pins for the analog and digital cores. The analog section is powered from the VA supply and the digital section is powered off of the VD supply. Both of these supply pins can be powered from the same external source with a small series resistor between them for noise isolation. Both the analog and digital cores can operate independently from 3.3 V to 5.0 V. The VL pin of the CS5340 supplies the digital interface logic, supports a wide operating range from 1.8 V to 5.0 V, and can be powered independently from the VA and VD power supplies.

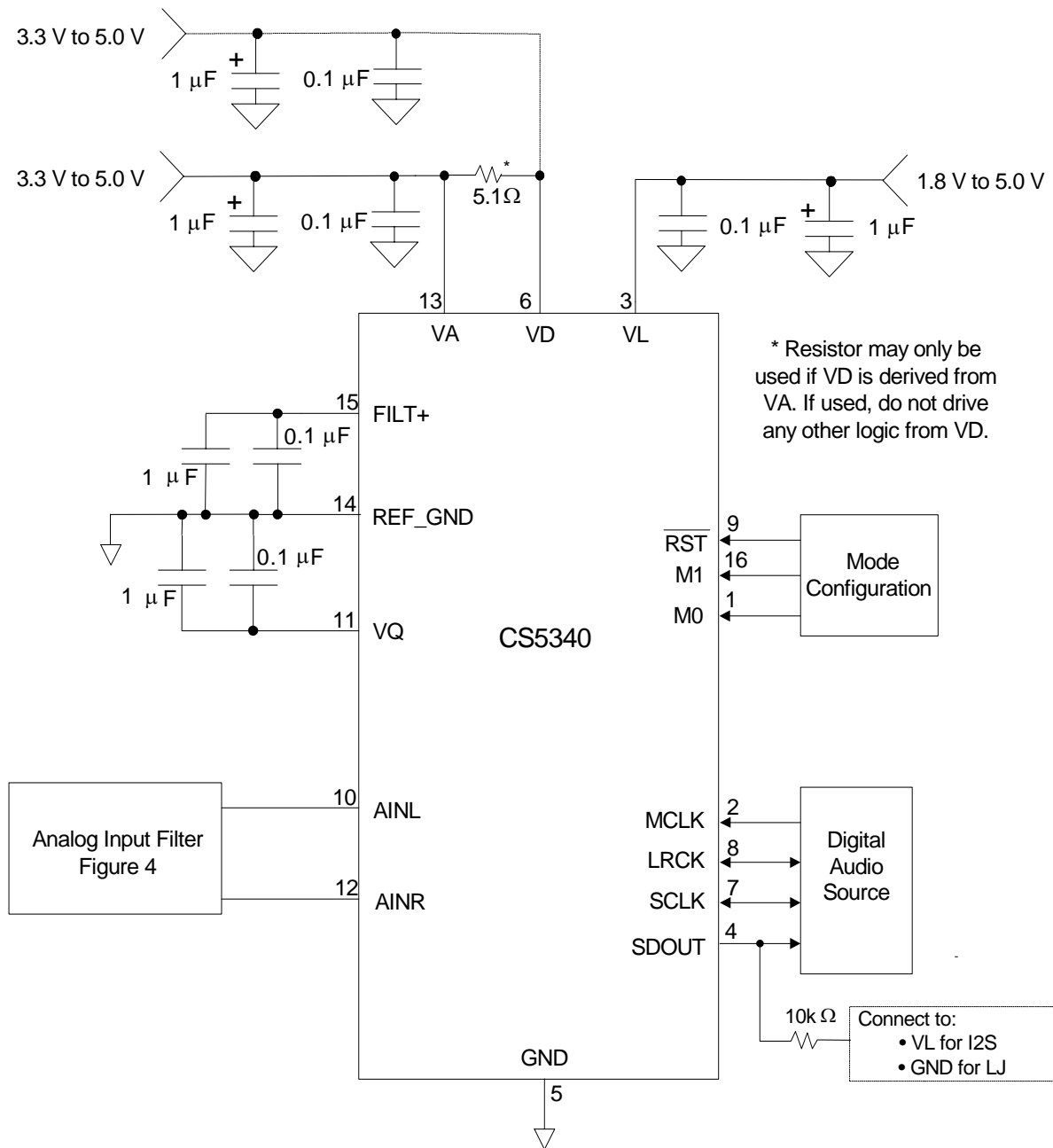


Figure 2. CS5340 Typical Connection Diagram

4. Master/Slave and Speed Mode Selection

4.1 CS5333

In the CS5333, the selection for Master or Slave mode operation is determined by a resistor pull-up/pull-down on the SDATA pin (pin 4), as noted in Figure 1. If operating in Master mode, the Speed mode is selected by the DIV pin (pin 8). If DIV is resistively pulled low, the CS5333 will enter into Base Rate mode ($F_s = 2 \text{ kHz to } 50 \text{ kHz}$). If DIV is resistively pulled high to V_L , the CS5333 will enter into High Rate mode ($F_s = 50 \text{ kHz to } 100 \text{ kHz}$). If the CS5333 is operating in Slave mode, the Speed mode is auto-detected and the DIV pin operates as an MCLK divide by two enable.

4.2 CS5340

In the CS5340, Master or Slave mode operation and Speed mode is determined by the mode pins, M1 and M0 (pins 16 and 1 respectively), as shown in Table 3.

M1 (Pin 16)	M0 (Pin 1)	Mode
0	0	Master, Single Speed Mode
0	1	Master, Double Speed Mode
1	0	Master, Quad Speed Mode
1	1	Slave, All Speed Modes

Table 3. CS5340 Mode Control

Please note that Base Rate mode is synonymous with Single Speed mode, and High Rate mode is synonymous with Double Speed mode.

5. Digital Interface Format Select

5.1 CS5333

The CS5333 supports both Left Justified and I^2S digital interface formats. The interface is selectable by the DIF pin (pin 9). If this pin is held at a logic low upon startup, I^2S interface format will be selected. If held at a logic high upon startup, Left Justified interface format will be selected.

5.2 CS5340

The CS5340 also supports both Left Justified and I^2S digital interface formats. The interface is selectable by a resistor pull-up/pull-down on the SDOOUT pin (pin 4). If this pin is resistively pulled low upon startup, Left Justified interface format will be selected. If this pin is resistively pulled high to V_L upon startup, I^2S interface format will be selected.

6. System Clocking

The clocking requirements for the CS5333 and CS5340 are the same for Master mode operation. However, in Slave mode operation the CS5340 only supports a subset of the clocking supported in the CS5333. The CS5333 supports an MCLK/LRCK ratio of 256x, 384x, 512x, and 768x in Base Rate mode and 128x, 192x, 256x and 384x in High Rate mode. The CS5340 cannot support ratios of 192x, 384x, or 768x. See Table 4. Due to the auto-speed mode detect circuitry implemented in the CS5340, not all sample rate ranges are supported in Slave mode. Please refer to the CS5340 datasheet for more information.

Device	Speed Mode	Supported MCLK/LRCK Ratios
CS5333	Base Rate	256, 384, 512, 768
	High Rate	128, 192, 256, 384
CS5340	Single Speed	256, 512
	Double Speed	128, 256

Table 4. Supported MCLK/LRCK Ratios, Slave Mode Operation

7. Input Filter Topology

Both the CS5333 and CS5340 implement a single-ended input architecture. Due to differences in the input sampling topologies within the converters, the input filter requirements are different between these two devices.

A suggested input filter topology for the CS5333 is shown in Figure 3. This input network consists of an AC-coupling capacitor along with a single-pole lowpass filter.

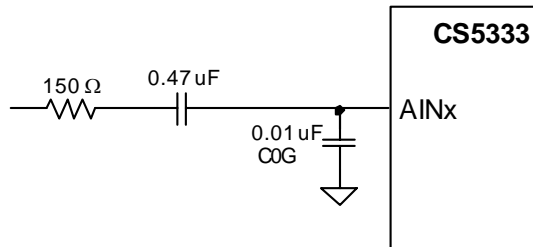


Figure 3. CS5333 Input Filter

The CS5333 will self-bias the analog input node to the optimal bias point (half of V_A). The CS5333 implements an internal buffer on the analog input, reducing the amount of switching current on the input sampling node. This reduction in switching current makes the CS5333 less sensitive to series resistance on the analog input lines.

A suggested input filter topology for the CS5340 is shown in Figure 4.

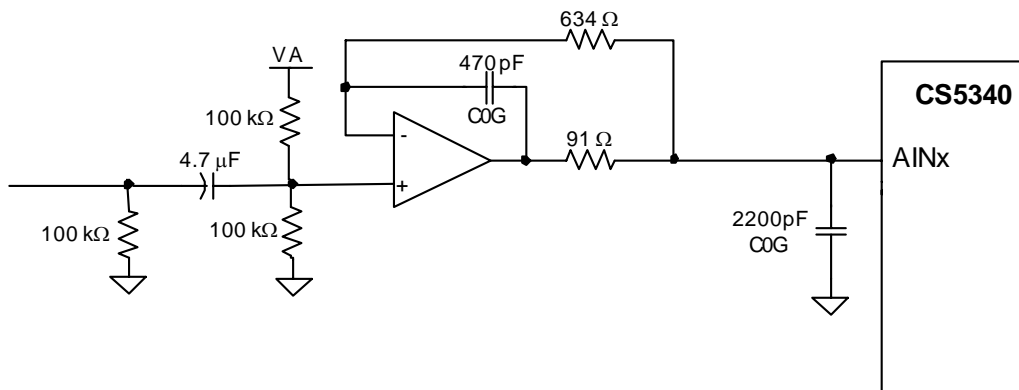


Figure 4. CS5340 Input Filter

This filter topology implements an external resistor-divider circuit to bias the output of the amplifier to the optimal bias point (half of V_A). Due to the internal architecture, the CS5340 requires low impedance on the analog input lines. The topology shown in Figure 4 provides a sub-ohm input source impedance into the CS5340 and isolates the input to the amplifier. For more information on this input filter topology, please refer to the Application Note AN241.

A passive input filter can be used with the CS5340, however, the full analog performance of the CS5340 will not be realized. Figure 5 illustrates a unity gain, passive input filter solution and the resulting distortion performance. Please note that in this case the dynamic range performance of the CS5340 will not be limited by the input filter; only the distortion performance is affected.

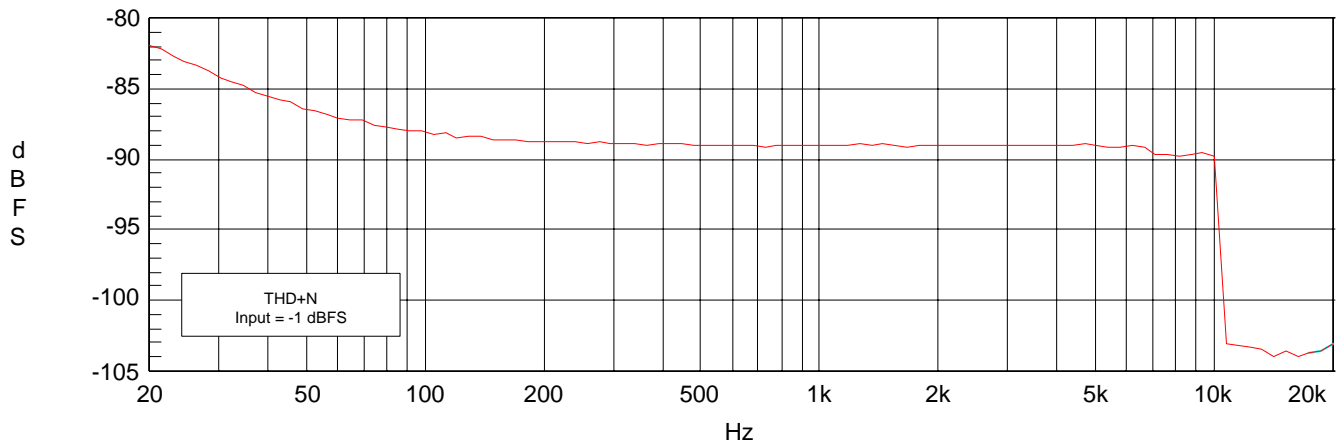
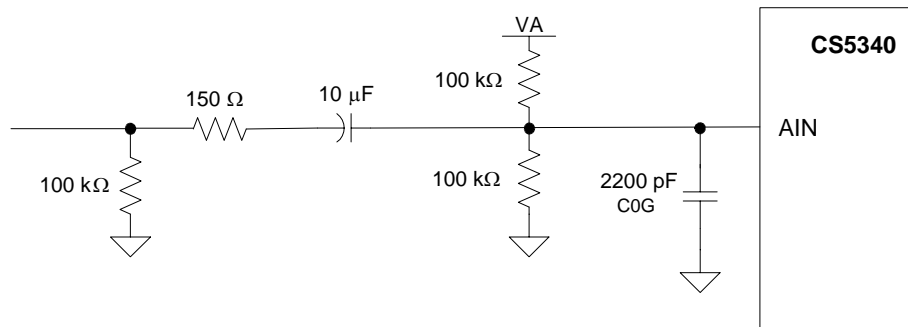


Figure 5. CS5340 Passive Input Filter, Solution 1

Some applications may require signal attenuation prior to the converter. The full-scale input voltage of the CS5340 will scale with the analog power supply voltage. For $V_A = 5.0\text{ V}$, the full-scale input voltage is approximately 2.8 Vpp , or 1 Vrms . Typical consumer audio line level outputs range from 1.5 to 2 Vrms . Figure 6 shows a passive input filter for the CS5340 and the resulting THD+N over the audio bandwidth. This filter provides 6 dB of signal attenuation. Due to the relatively high input impedance on the CS5340 analog inputs, the full distortion performance of the CS5340 cannot be realized. Also, the combination of the series resistor and the biasing resistor-divider circuit will determine the input impedance into the input filter. In the circuit shown in Figure 6, the input impedance is approximately $5\text{ k}\Omega$. By doubling the resistor values, the input impedance will increase to $10\text{ k}\Omega$. However, in this case the distortion performance will drop to approximately 70 dB due to the increase in series resistance on the CS5340 analog inputs.

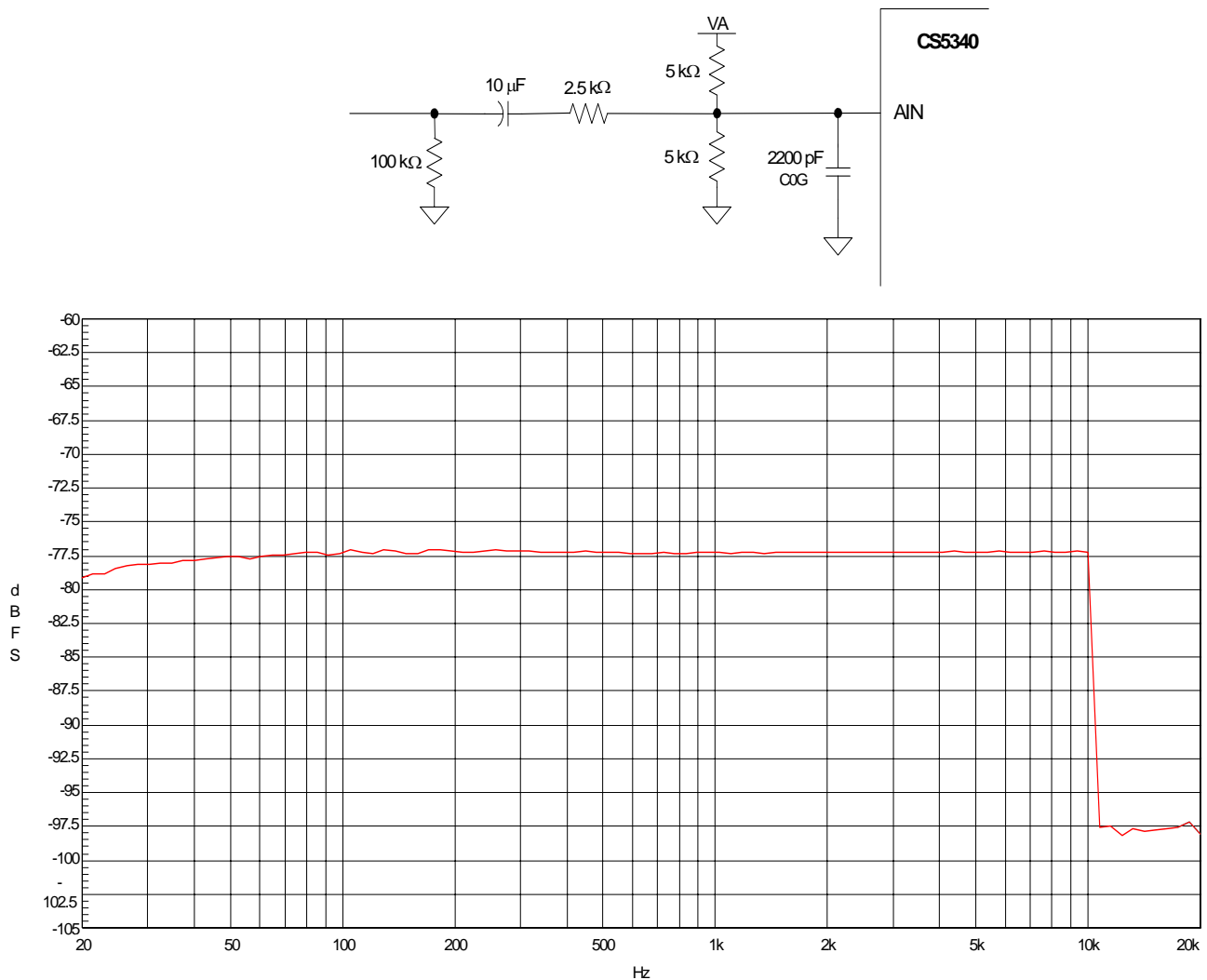


Figure 6. CS5340 Passive Input Filter, Solution 2

8. Capacitor Size on the Reference Pin (FILT+)

The CS5340 and CS5333 require external capacitance on the internal reference voltage pin. For the CS5333, the internal reference voltage is output on FILT+ (pin 11). On the CS5340, the FILT+ reference voltage is output on pin 15. The size of the decoupling capacitor on this reference pin will affect the low frequency distortion performance. The recommended solution for the CS5333 is a 1 μF capacitor between the FILT+ pin and analog ground. The recommended solution for the CS5340 is to use a 0.1 μF capacitor in parallel with a 1 μF capacitor for cost sensitive applications. See Figure 7 which illustrates the typical low frequency distortion performance of the CS5340 with different size capacitors on the FILT+ reference pin (pin 15). This plot was taken implementing the recommended input filter shown in Figure 4.

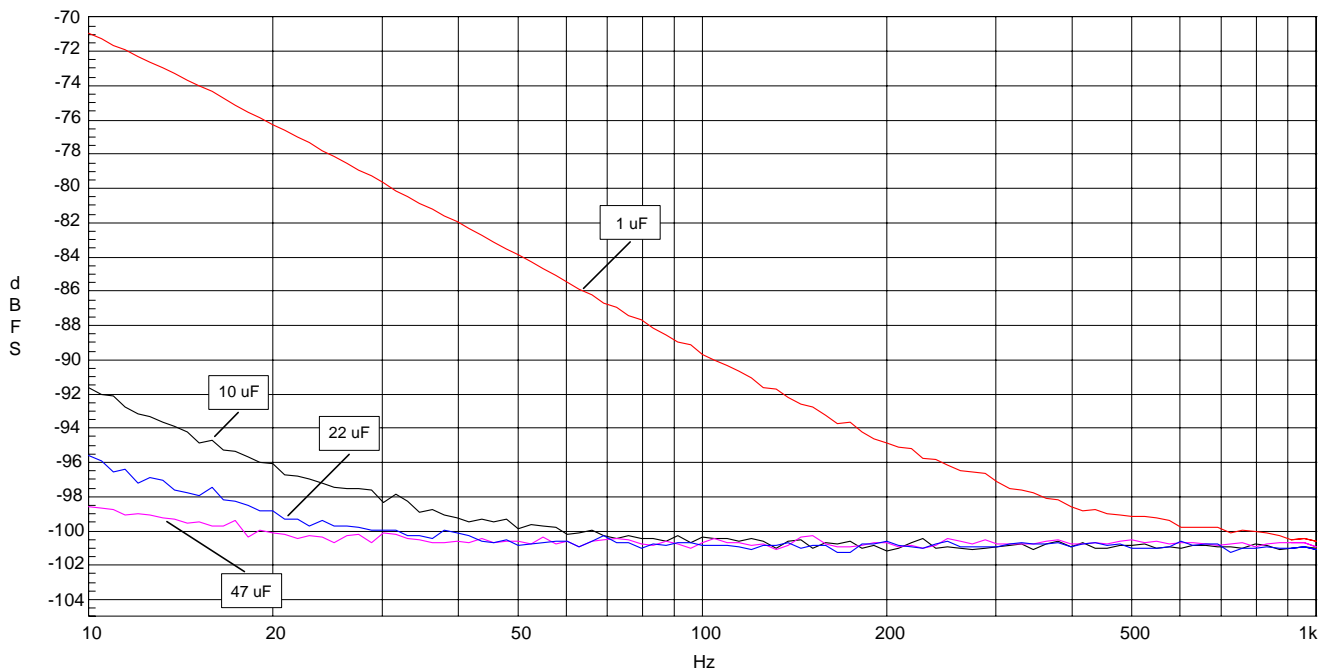


Figure 7. CS5340 THD+N versus Frequency

9. Conclusion

The CS5340 is the recommended replacement for the CS5333, offering higher performance and 192 kHz output sample rate capability. Special considerations must be made when upgrading designs to use the CS5340 in place of the CS5333. These considerations include pin compatibility, functional mode selections, input filter design, and external capacitor requirements on the FILT+ reference pin.

Revision	Date	Change
1	16 March 2004	Initial Release

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